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RF PA predistortion using Non-Linear RF-DACs

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Summary

Predistorters, analog or digital, may be used to linearize power amplifiers (PAs) at the cost of additional hardware. We here present a novel linearization scheme which uses segmented non-linear RF-DACs to linearize PAs at no additional hardware cost. We also show that the non-linear expanding DAC characteristic may be adjusted, allowing for the linearization to be adopted.

1 Introduction

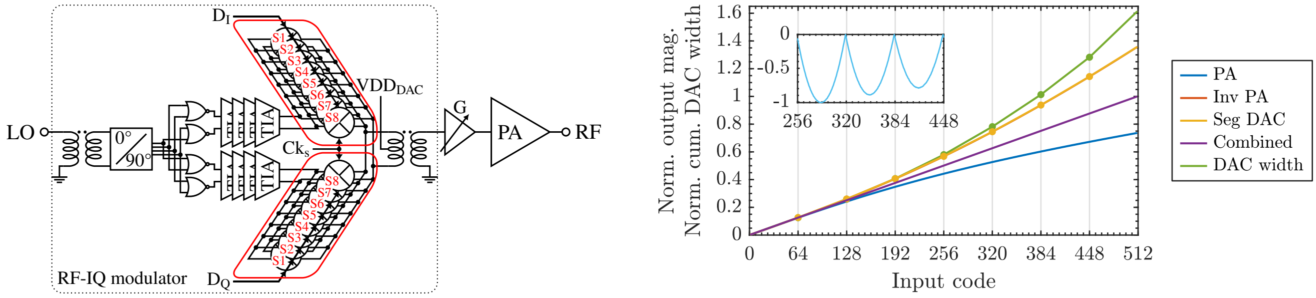
Power amplifiers (PAs) are used to extend the output power when the capabilities of the IQ-modulator is not sufficient. However, with the inverse relationship between linearity and efficiency, PAs need to operate in significant power back-off to fulfill the linearity requirements, or a predistorer (PD) is needed. There are both analog PDs (APDs) [1] and digital PDs (DPDs) [2], both requiring additional hardware for performing the linearization. In this abstract, we present a novel linearization approach which utilizes non-linearly scaled RF-DACs to compensate for the non-linearities of the combined RF-DAC and PA driven by it.

2 Linearization

A schematic of the transmitter concept is shown in Fig. 1a. Non-overlapping LO signals are generated and fed to two segmented non-linear RF-DACs, followed by a gain stage and finally the PA. The RF-DACs are based on the topology presented in [3] and modelled using a 22 nm FDSOI CMOS process. The PA uses a stacked configuration and is modelled in the same technology as the RF-DACs. In Fig. 1b, we show the PA characteristic and its inverse together with the output from the segmented non-linear DAC. For a linear code to PA output mapping, the output from the DAC should realize the inverted PA characteristic. Since the DAC also will experience compression, the expanding segmented non-linear scaling must be more aggressive than the inverted PA characteristic alone (see the normalized cumulative DAC width in Fig. 1b) to compensate for the joint compression of both the DAC and the PA. Although the DAC scaling is fixed in hardware, the RF-DAC bias enables adjustments of the transfer characteristic. Since the DAC compression is dependent on the DAC bias settings and since this compression counteracts the expanding non-linear scaling, the DAC transfer characteristic may be adapted to approximate the inverse DAC plus PA characteristic. Figure 2 shows the output magnitude normalized (using the highest code) to the design point (the blue curve) versus input code, for both DAC and DAC plus PA. The effect of an increased DAC supply voltage is shown for a fixed LO magnitude in Figs. 2a and 2b and for an increased LO magnitude with a fixed DAC supply voltage in Figs. 2c and 2d.

3 Evaluation

The proposed linearization concept has been evaluated through individual schematic-level circuit simulations of the key components: RF-DACs (excluding the LO generation) and PA. All simulations are based on the dominating quasi-static behaviour,



(a) (b)

Figure 1. (a) A schematic showing the transmitter concept used as the base for the evaluation. (b) The PA characteristic, its inverse, the segmented scaling, the resulting output from the cascaded DAC and PA, and the normalized cumulative DAC width. The inset shows the difference between the output from the segmented DAC and the inverted PA characteristic.

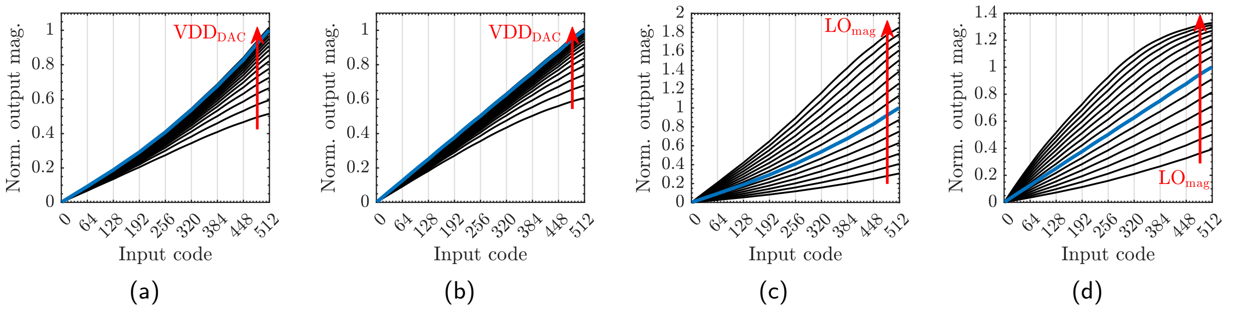


Figure 2. Normalized output magnitude (a) for DAC versus supply voltage, (b) for DAC combined with PA versus supply voltage, (c) for DAC versus LO magnitude, and (d) for DAC combined with PA versus LO magnitude. The curves are normalized (using the highest code) relative to the design point, the blue curve.

hence the signal bandwidth has no effect. With non-overlapping LO signals, the cross-modulation distortion can be kept small [3], making it possible to combine two individually simulated RF-DACs into a Cartesian modulator. This Cartesian configuration was used to evaluate linearization performance for modulated 256QAM single-carrier (SC) signals, up-sampled 4 times using an RRC-filter. In Figs. 3a and 3b, the static performance (rms linearity and maximum phase variation) is presented for different DAC bias conditions. The red contours indicate the PA compression for each bias point and the white diamond marks the nominal design point. In Figs. 3c and 3d, the modulated performance (EVM and ACPR) is presented for different DAC bias conditions. The shallower and slightly shifted optimum observed for modulated signals is caused by the 1D linearization that results when applying the expanding non-linearity on each quadrature component individually, giving slightly degraded linearization performance for symbols in the constellation corners.

The proposed linearization concept only uses increased unit cell transistor widths. This in contrast to APDs and DPDs which require additional hardware in the analog or digital domain. Although the evaluation has been performed using a Cartesian IQ-modulator, the same principles can also be applied to a system using a polar IQ-modulator. More results are available in [4].

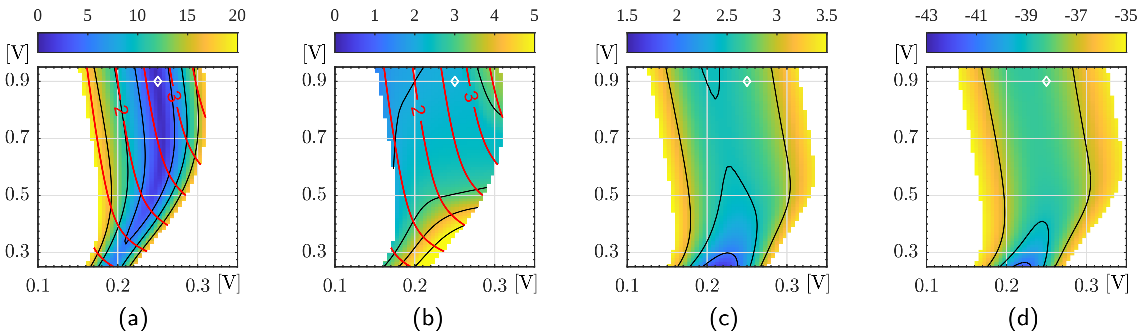


Figure 3. Static performance ((a) RMS linearisy [LSB], (b) maximum phase variation [°]) and modulated performance ((c) EVM [%], (d) ACPR [dBc]) versus DAC supply voltage [V] (vertical) and LO magnitude [$V_{pk\text{-}pk}$] (horizontal). Red contours indicate PA compression in dB. Diamond marker highlights the nominal design point.

4 Acknowledgements

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